Design Problems

NOTE: All models developed for this assignment should be of adequate quality to be used in your final CPU design.

Pb A [45 pts]
Design a Register File module that has the following format:

```
module RF(rreg1_addr, rreg2_addr, wreg_addr, din, wreg, clk, dout1, dout2);
  input [4:0] rreg1_addr, rreg2_addr; // addresses of registers to be read
  input [4:0] wreg_addr; // address of register to write into
  input [31:0] din; // data to be written into register addressed by wr_addr
  input wreg; // control signal (data is written only when this signal is enabled)
  input clk; // clock
  output [31:0] dout1, dout2; // values read from registers rreg1_addr and rreg2_addr
endmodule
```

Choose a few test cases that demonstrate the vital aspects of the implementation and submit your simulation output along with the RTL style VHDL code for RF, and the associated VHDL TB code.

Pb. B [55]
Design a Memory behavioral module (doesn't need to be synthesizable) that has the following format:

```
module Memory(addr, din, mr, mw, clk, dout);
  input [6:0] addr; // 7-bit address to memory.
  input [31:0] din; // data to be written into Memory
  input mr; // data in memory location addr is read if this control is set
  input mw; // din is written in addr during positive clock edge if this control is set
  input clk;
  output [31:0] dout; // value read from memory location addr
endmodule
```

Choose a few test cases that demonstrate the vital aspects of the implementation and submit your simulation output along with the RTL style VHDL code for RF, and the associated VHDL TB code.

Grading will be based on the following criteria:

- Correctness of the design [40 %]
- Compliance with specification [10 %]
- Coding style [20 %]
- Effectiveness of testing [30 %]