Design Problems

NOTE: All models developed for this assignment should be of adequate quality to be used in your final CPU design.

Pb. A. [30 pts]
Design a 32-bit ALU as shown below. This is the 32-bit ALU model that you will use in your processor final design. The model must have the following format.

```vhdl
Module ALU32(a, b, op, result, set, zero);
  input [31:0] a, b;
  input [2:0] op; // op[2] is "b invert ".
  // op[1:0] denotes the 2-bit operation.
  output [31:0] result;
  output set; // set is the result of the most-significant ADDER unit.
  output zero; // zero is 1 if the result is 0x0000. Otherwise, it is 0.
```

Submit the RTL style VHDL code for the 32-bit ALU.
Submit and explain the waveforms used for testing.

Pb. B [5 pts]
Design a 16 to 32-bit sign extension unit. The module must have the following format.

```vhdl
module SignExtend(a, result);
  input [15:0] a;  // 16-bit input
  output [31:0] result; // 32-bit output
```

Submit the RTL style VHDL code for the Sign Extension Unit.
Submit and explain the waveforms used for testing.

Pb. C [15 pts]
Design a new 32-bit ALU that puts together your previously designed ALU32 and Overflow modules. The model must have the following format.

```vhdl
module ALU(a, b, op, result, set, zero, ov);
  input [31:0] a, b;
  input [2:0] op; // op[2] is "b invert ".
  // op[1:0] denotes the 2-bit operation.
  output [31:0] result;
  output set; // set is the result of the most-significant ADDER unit.
  output zero; // zero is 1 if the result is 0x0000. Otherwise, it is 0.
  output ov;    // overflow
```

Submit the structural style VHDL code for ALU.
Submit and explain the waveforms used for testing.

Grading will be based on the following criteria:
- Correctness of the design [40 %]
- Compliance with specification [10 %]
- Coding style [20 %]
- Effectiveness of testing [30 %]