ENGR430 – CMOS INTEGRATED CIRCUITS DESIGN  
(FALL 2006)

INSTRUCTOR: Claudio Talarico  
OFFICE: CEB (Computer & Engineering Bldg.), Room 336  
OFFICE HOURS: MW 10:00 am -1:00 pm, and by appointment.  
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COURSE URL: http://www.ewu.edu/x30360.xml

CLASS LOCATION AND SCHEDULE:  
M, W  8:00-9:40, CEB 231  
T  8:00-9:40, CEB 232 (Lab.)

COURSE DESCRIPTION:  
The aim of this course is to provide students with the theoretical and practical knowledge required for analyzing and designing very large scale integration (VLSI) circuits and systems in Complementary Metal-Oxide-Semiconductor (CMOS) technology. Lab. includes hands-on use of a variety of state of the art CAD tools and design techniques.

LEARNING OBJECTIVES:  
Upon completion of this course, students will be able to:  
1. Analyze and design basic logic circuits that form the building blocks of a digital integrated system particularly with applications to combinational logic gates and sequential logic gates (ABET criteria 3a, 3c)  
2. Use CAD tools to layout the physical structure of various basic circuits (ABET criteria 3j, 3k)  
3. Evaluate the chip area required to layout different logic circuits (ABET criteria 3a, 3b)  
4. Use circuit simulation (SPICE) to verify the functionality of basic logic circuits (ABET criteria 3j, 3k)  
5. Use circuit simulation (SPICE) to analyze and improve the performance metrics of basic logic circuits (ABET 3b, 3k)  
6. Explain Layout Design Rules for CMOS Processing Technology (ABET 3i, 3j)  
7. Model and estimate the propagation delay of CMOS gates (ABET 3a, 3c)  
8. Estimate CMOS chips power dissipation (ABET 3a, 3j)  
9. Explain the role of design margin and reliability (ABET 3h, 3i, 3j)  
10. Estimate the effect of scaling a CMOS technology on system performance (ABET 3i, 3j)  
11. Explain the concepts of setup-time, hold-time, clock skew, max-delay constraints, and min-delay constraints (ABET 3a, 3j)  
12. Calculate the critical path delay of a synchronous digital system (ABET 3a, 3c, 3e)  
13. Outline design methodologies and strategies for digital integrated circuits (ABET 3e, 3h, 3i, 3j, 3k)  
14. Model combinational logic and sequential logic using VHDL (ABET 3e, 3g, 3j, 3k)  
15. Use various CAD tools (design entry, synthesis, static timing analysis, simulation, verification and layout) for the open ended design of a digital integrated system or sub-system (ABET 3e, 3g, 3i, 3j, 3k)

TEXTBOOK:  

PREREQUISITES:  
ENGR 160 (Digital Circuits), and ENGR 330 (Electronics I) or consent of the instructor.
**Grading:**

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<th>Component</th>
<th>Percentage</th>
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<tr>
<td>Homework</td>
<td>20%</td>
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<td>Labs</td>
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<td>Midterms</td>
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<td>Final</td>
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<td>B</td>
<td>3.0-3.4</td>
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<td>C</td>
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<td>D</td>
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Late work will **NOT** be accepted.

**Course Contents:**
- Introduction to CMOS Technology and Integrated Circuits Design
- MOS Transistor Theory
- CMOS Technology
- Circuit Characterization and Performance Estimation
- Circuit Simulation
- Combinational Circuit Design
- Sequential Circuit Design
- Design Methodology and Tools
- Hardware Description Languages and Logic Synthesis (VHDL)