Number: ENGR 430 (Section 01)

Title: CMOS (Complementary Metal Oxide Semiconductor) Integrated Circuits Design

Credits: 5 credits

Course Format: Two two-hour lectures per week. One two-hour lab. per week.

Coordinator: Claudio Talarico, Ph.D., Assistant Professor
Computer Engineering Building, Room 336
e-mail: ctalarico@ewu.edu Tel.: 509-359-4780

Catalog Description:
The aim of this course is to provide students with the theoretical and practical knowledge required for analyzing and designing very large scale integration (VLSI) circuits and systems in Complementary Metal-Oxide-Semiconductor (CMOS) technology. Lab. includes hands-on use of a variety of state of the art CAD tools and design techniques.

Learning Objectives (and corresponding mapping to ABET Criteria 3):
Upon completion of this course, students will be able to:
1. Analyze and design basic logic circuits that form the building blocks of a digital integrated system particularly with applications to combinational logic gates and sequential logic gates (ABET criteria 3a, 3c)
2. Use CAD tools to layout the physical structure of various basic circuits (ABET criteria 3j, 3k)
3. Evaluate the chip area required to layout different logic circuits (ABET criteria 3a, 3b)
4. Use circuit simulation (SPICE) to verify the functionality of basic logic circuits (ABET criteria 3j, 3k)
5. Use circuit simulation (SPICE) to analyze and improve the performance metrics of basic logic circuits (ABET 3b, 3k)
6. Explain Layout Design Rules for CMOS Processing Technology (ABET 3i, 3j)
7. Model and estimate the propagation delay of CMOS gates (ABET 3a, 3c)
8. Estimate CMOS chips power dissipation (ABET 3a, 3j)
9. Explain the role of design margin and reliability (ABET 3h, 3i, 3j)
10. Estimate the effect of scaling a CMOS technology on system performance (ABET 3i, 3j)
11. Explain the concepts of setup-time, hold-time, clock skew, max-delay constraints, and min-delay constraints (ABET 3a, 3j)
12. Calculate the critical path delay of a synchronous digital system (ABET 3a, 3c, 3e)
13. Outline design methodologies and strategies for digital integrated circuits (ABET 3e, 3i, 3j, 3k)
14. Model combinational logic and sequential logic using VHDL (ABET 3e, 3g, 3j, 3k)
15. Use various CAD tools (design entry, synthesis, static timing analysis, simulation, verification and layout) for the open ended design of a digital integrated system or sub-system (ABET 3e, 3g, 3i, 3j, 3k)

Textbooks: N.H.E. Weste, D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison-Wesley 3/e, 2004

Prerequisites: ENGR 160 (Digital Circuits), and ENGR 330 (Electronics I) or consent of the instructor.
Topics:
- MOS Transistor
- CMOS Technology
- CMOS Circuits Characterization and Performance Estimation
- CMOS Circuits Design and Simulation
- Design and Analysis of Digital Systems
- Design Methodologies and Tools
- Hardware Description Languages and Logic Synthesis

Computer Usage:
1. Extensive CAD tool use: Design Entry, Simulation, Synthesize, Layout, and Verification.
2. Design projects and laboratory assignments involving formal technical reports requires the use of word processing and graphics software for their presentation.

Laboratory:
Laboratory experiments and design projects require an understanding of basic CMOS digital circuit analysis and design and involve the use of CAD tools, personal computers, UNIX servers, writing skills and teamwork.

Grading:
\[
\begin{align*}
A &= 3.5–4.0 \ (90–100\%), \\
B &= 3.0–3.4 \ (80–89\%), \\
C &= 2.0–2.9 \ (70–79\%), \\
D &= 1.0–1.9 \ (60–69\%), \\
F &= 0.0 \ (0–59\%)
\end{align*}
\]

Assignments: 20%
Labs 20%
Midterm exam: 30%
Final exam/project: 30%

Course Outcomes and mapping to ABET Criteria 3:

a. An ability to apply knowledge of mathematics, science, and engineering.
   Students are required to use their background in mathematics, physics and engineering to successfully finish homework, labs, and exams.

b. An ability to design and conduct experiments, as well as to analyze and interpret data.
   Students are required to design and implement lab experiments for analyzing, designing, and improving CMOS circuits and systems.

c. An ability to design a system component, or process to meet desired needs within realistic constraints.
   Homework, laboratory experiments, and an open ended project require students to analyze, design, evaluate, and improve CMOS digital systems that must meet specified constraints.

d. An ability to function effectively on multi-disciplinary teams.
   n/a

e. An ability to identify, formulate, and solve engineering problems
   An open-ended project requires students to identity, formulate, model and solve several engineering challenges.

f. An understanding of professional and ethical responsibility.
   n/a

g. An ability to communicate effectively.
   Students need to write lab. reports, and an open-ended project’s proposal, specification, and documentation.

h. Understand impact of engineering solutions in a global, economic, environmental and societal context
   n/a
i. *A Recognition of the need for, and an ability to engage in life-long learning*
   Students must plan the design and development of an open-ended project and self-learn several CAD tools.

j. *A Knowledge of contemporary issues*
   Homework, lab. experiments, and open-ended project are based on state of the art CMOS technologies

k. *An ability to use the techniques, skills and modern engineering tools necessary for engineering practice.*
   Lab. experiments and the open-ended project require the use current methodologies and CAD tools.

**Prepared by:** Claudio Talarico  
**Last Revised:** June, 24, 2006