The following assignments address Course Learning Objective #8 and Course Learning Objective #4.

Use various CAD tools for the open ended design of a digital integrated system or sub-system (ABET criteria 3e, 3g, 3i, 3j, 3k)

Use circuit simulation (SPICE) to analyze and improve the performance metrics of basic logic circuits (ABET criteria 3b, 3k)

Assignment:
Use AMI C5 process to develop a CMOS standard cell library composed by the following core logic cells:

- 2 input nand gate
- Inverter
- 2:1 mux
- D flip flop
- D flip flop with clear

Use LT spice to draw the schematic of each cell and for characterizing their behavior.

Write a “professional” quality report containing:
1. A data sheet for each of the cells implemented.

Collaboration between groups is strongly encouraged!!

The logic cells should be named after the AMI 0.5μ Standard Cell Core Library.

Logic Cells
NA21, INV1, MX21, DF001, DF111,