The following assignments address Course Learning Objective #8 and Course Learning Objective #4.

Use various CAD tools for the open ended design of a digital integrated system or sub-system (ABET criteria 3e, 3g, 3i, 3j, 3k)

Use circuit simulation (SPICE) to analyze and improve the performance metrics of basic logic circuits (ABET criteria 3b, 3k)

Assignment A

Design a CMOS inverter using OnSemi C5 technology (†). Assume the inverter is driving a capacitive load $C_L$. Simulate the circuit to verify it functions correctly, and measure the rise time, fall time and propagation delay (time it takes from the 50% of the input voltage final value to the 50% of the output voltage final value) for three capacitive loading scenarios: $C_L=1\text{fF}, 10\text{fF}, 50\text{fF}$. Do not forget to specify $L$ and $W$ for the two transistors.

Write a short report showing:
1. LTspice schematic
2. Associated spice deck
3. Any relevant simulation waveform
4. The values of $t_{\text{rise}}, t_{\text{fall}}, t_{\text{pd}}$ for all three loading scenarios

Assignment B

Modify your previous schematic to include an inductor of 50 nH between VDD and the pull-up transistor of your inverter. What happen to the output voltage?

Add to the report:
1. Modified LTspice schematic
2. Associated spice deck,
3. Output voltage waveforms
4. A short qualitative explanation of why the output voltage changes as observed

Assignment C

Modify your schematic one more time to include a 100 nF capacitor between the source of the pull-up transistor and ground. What happen to the output voltage?

Add to the report:
1. Modified LTspice schematic
2. Associated spice deck,
3. Output voltage waveforms
4. A short qualitative explanation of why the output voltage changes as observed

**HINT (*):**
Use the SPICE transistor models for the typical corner case. OnSemi C5 SPICE models (BSIM 3v3) are provided on the course website, however you have to change the SPICE level to the correct value required for LTSPICE (check LTSPICE manual). Make sure to use realistic values for the transistors’ s length and width (look at the OnSemi C5 test data provided on the course website)