ENGR 430 – Lab. #3

The following assignments address Course Learning Objective #8 and Course Learning Objective #4.

Use various CAD tools for the open ended design of a digital integrated system or sub-system (ABET criteria 3e, 3g, 3i, 3j, 3k)

Use circuit simulation (SPICE) to analyze and improve the performance metrics of basic logic circuits (ABET criteria 3b, 3k)

Assignment:
Use AMI C5 process to develop a CMOS standard cell library composed by three core logic cells of your choice (provided that two are combinational cells and one is a sequential cell) among the following:

- 2 input nand gate
- 2 input nor gate
- Inverter
- Tri-state inverter
- 2:1 mux
- D flip flop
- D flip flop with clear

Use LT spice to draw the schematic of each cell and for characterizing their behavior.

Write a “professional” quality report containing:
1. A data sheet for each of the cells implemented.

Collaboration between groups is strongly encouraged!!

The logic cells should be named after the AMI 0.5µ Standard Cell Core Library.

<table>
<thead>
<tr>
<th>Logic Cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>NA21, NO21, INV1, ITB1, MX21, DF001, DF111,</td>
</tr>
</tbody>
</table>