ENGR 430 – Lab. #2

The following assignment addresses Course Learning Objective #8.

*Use various CAD tools for the design of a digital integrated system or sub-system (ABET criteria 3e, 3g, 3i, 3j, 3k)*

**Assignment A**

Given an RC circuit which input is a voltage step from 0 to 5V, and which output is the voltage on the capacitor, derive the circuit delay time (time it takes the output voltage to reach the 50% of its final value), and the circuit rise time (time it takes the output voltage to go from the 10% to the 90% of its final value).

Verify your derivations are consistent with LT Spice simulator.

Write a short report showing:

1. Detailed derivations of delay and rise time
2. LTspice schematic
3. Associated spice deck
4. Any relevant simulation waveform.

**Assignment B**

Modify your previous schematic to include a switch. Assume the switch is initially open and the capacitor is initially charged at 2V. The switch closes at t=2ns.

Add to the report:

1. Modified LTspice schematic
2. Associated spice deck,
3. Input and output voltage simulation waveforms.