The following assignments address Course Learning Objective #6.

Model and Estimate the propagation delay of CMOS gates (ABET criteria 3a, 3c)

- Ex. 2.10 p. 109

The following assignment addresses Course Learning Objective #7.

Explain the role of design margin and reliability (ABET criteria 3i, 3j)

- Ex. 2.14 p. 110
- Ex. 2.21 p. 111