ENGR 430 – Homework #2

The following assignments address Course Learning Objective #2.

Evaluate the chip area required to layout different logic circuits (ABET criteria 3a, 3b)

- Ex. 1.8 p. 64
- Ex. 1.9 p. 64

The following assignment addresses Course Learning Objective #1.

Analyze and design basic logic circuits that form the building blocks of a digital integrated system particularly with applications to combinational logic gates and sequential logic gates (ABET criteria 3a, 3c)

- Ex. 1.13 p.64