library IEEE;
use IEEE.std_logic_1164.all;
entity two_phase is
port(phi1, phi2, reset: out std_logic);
end entity two_phase;

architecture behavioral of two_phase is
begin
  rproc: reset <= '1', '0' after 10 ns;
  clock_process: process is
  begin
    phi1 <= '1', '0' after 10 ns;
    phi2 <= '0', '1' after 12 ns,
           '0' after 18 ns;
    wait for 20 ns;
  end process clock_process;
end architecture behavioral;

Note the “perpetual” behavior of processes