VHDL Design Organization

- **Entity**
  the “symbol” interface (input/output ports)

- **Architecture**
  one of the several possible implementation of the design

- **Configuration**
  binding between the symbol and one of the many possible implementation. Can be used to express hierarchy.
Register Transfer Level

- Only a small subset of the Language statements can be mapped into “Silicon”.

```
X <= (A AND B) OR X1;
X1 <= (X3 XOR G)
X2 <= (X OR NOT F)
X3 <= (C AND X2)
```