Hardware Description Languages

Modeling Structure
Elements of structural models

- Structural models describe a digital system as an interconnection of components
- An entity/architecture for each component must be independently available
Structural models

- Structural models are always “built” as follows:
  - Define the components used in the design
  - Describe the interconnection of these components

- Structural models can be easily generated (automatically) from schematics

- Structural descriptions can be nested
Hierarchy and Abstraction

- Structural modeling expresses the hierarchical nature of designs and provides a mechanism for the instantiation and reuse of cores
An example of structural modeling (1)
library ieee;
use ieee.std_logic_1164.all;

entity shiftcomp is port(
    Clk, Rst, Load: in std_logic;
    Init: in std_logic_vector(0 to 7);
    Test: in std_logic_vector(0 to 7);
    Limit: out std_logic);
end shiftcomp;
architecture structure of shiftcomp is

    component compare
        port(A, B: in std_logic_vector(0 to 7);
            EQ: out std_logic);
    end component;

    component shifter
        port(Clk, Rst, Load: in std_logic;
            Data: in std_logic_vector(0 to 7);
            Q: out std_logic_vector(0 to 7);
            Qb: out std_logic_vector(0 to 7));
    end component;

    signal Q_net: std_logic_vector(0 to 7);

begin

    COMP_1: compare port map (A => Q_net, B => Test,
                                EQ => Limit);
    SHIFT_1: shifter port map (Clk => Clk, Rst => Rst,
                                Load => Load, Data => Init,
                                Q => Q_net, Qb => open);

end structure;
-- 8-bit barrel shifter

library ieee;
use ieee.std_logic_1164.all;

entity shifter is
  port(
    Clk, Rst, Load: in std_logic;
    Data: in std_logic_vector(0 to 7);
    Q: out std_logic_vector(0 to 7);
    Qb: out std_logic_vector(0 to 7)
  );
end shifter;

architecture rtl of shifter is
begin
  reg: process(Rst,Clk)
  variable Qreg: std_logic_vector(0 to 7);
  begin
    if Rst = '1' then   -- Async reset
      Qreg := "00000000";
    elsif rising_edge(Clk) then
      if Load = '1' then
        Qreg := Data;
      else
        Qreg := Qreg(1 to 7) & Qreg(0);
      end if;
    end if;
  Q  <= Qreg;
  Qb <= not(Qreg);
  end process;
end rtl;
An example of structural modeling (5)

```vhdl
-- Eight-bit comparator

library ieee;
use ieee.std_logic_1164.all;

entity compare is
  port( A, B: in std_logic_vector(0 to 7);
       EQ  : out std_logic);
end compare;

architecture rtl of compare is
begin
  EQ <= '1' when (A = B) else '0';
end rtl;
```