An example of structural modeling (1)
An example of structural modeling (2)

library ieee;
use ieee.std_logic_1164.all;

entity shiftcomp is port(
  Clk, Rst, Load: in std_logic;
  Init: in std_logic_vector(0 to 7);
  Test: in std_logic_vector(0 to 7);
  Limit: out std_logic);
end shiftcomp;
architecture structure of shiftcomp is

   component compare
       port(A, B: in std_logic_vector(0 to 7);
            EQ: out std_logic);
   end component;

   component shifter
       port(Clk, Rst, Load: in std_logic;
            Data: in std_logic_vector(0 to 7);
            Q: out std_logic_vector(0 to 7);
            Qb: out std_logic_vector(0 to 7));
   end component;

   signal Q_net: std_logic_vector(0 to 7);

begin

   COMP_1: compare port map (A => Q_net, B => Test,
                                EQ => Limit);
   SHIFT_1: shifter port map (Clk => Clk, Rst => Rst,
                                Load => Load, Data => Init,
                                Q => Q_net, Qb => open);

end structure;