HDL coding Styles

- Register Transfer Level
- Structural
- Behavioral

Be careful NOT everybody gives the same meaning to the term BEHAVIORAL!

HDL applications

- High Level Modeling (Behavioral style)
- Design Entry (Structural & RTL styles)
- Simulation (Behavioral style)
  - Validation by mean of a test bench

```vhdl
// dut_tb.vhd
// instantiate design to test
// observe responses
```

TESTBENCH
Levels of Abstraction

- Behavioral
- RTL
- Structural

Behavioral Level

- Describe behavior (functionality and performances)
- All language features can be used
Register Transfer Level

- Only a small subset of the Language statements can be mapped into “Silicon”.

![Diagram of Register Transfer Level]

Structural Level

- Sub-Modules interconnection
- Primitive cells interconnection (net-list)
- The code describes a bunch of port mappings.

![Diagram of Structural Level]