Number: ENGR 465
Title: Hardware Description Languages
Credits: 4 credits

Course Format: Three hours of lecture and two hours of lab per week.

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Catalog Description:
This course introduces methodologies and computer-aided design (CAD) tools for the design of complex electronic systems. Emphasis is on high-level description languages and their use for specifying, designing, simulating and synthesizing digital VLSI circuits in MOS (metal-oxide-semiconductor) technologies. Special attention will be devoted to VHDL. Theoretical knowledge will be complemented by hands-on use of several commercial CAD tools.

Learning Objectives and Corresponding Mapping to ABET Criteria 3: Upon completion of this course, students will be able to:

1. Demonstrate proficiency coding in HDL (Hardware Design Language). (Criteria 3a, 3e, 3j, 3k)
2. Design basic functional units with HDL. (Criteria 3a, 3b, 3c, )
3. Design advanced application specific function units with HDL. (Criteria 3a, 3b, 3c, 3i, 3j, 3k)
4. Demonstrate how to map a design described in HDL into FPGA (Field Programmable Gate Array. (Criteria 3i, 3j, 3k)
5. Apply HDL to various application problems. (Criteria 3b, 3c, 3e, 3g, 3k)

Textbooks: V.A. Pedroni, Circuit Design with VHDL, MIT Press, 2004

Prerequisites: ENGR 160 (Digital Circuits) or consent of the instructor.

Topics:
- Combinational and sequential circuits with schematic diagrams.
- Combinational and sequential circuits with VHDL.
- Design entry of complex digital systems with VHDL
- Simulation of complex digital systems with VHDL
- Synthesis of complex digital system with VHDL and FPGA

Computer Resources: Computers with Xilinx software.

Laboratory:
Laboratory experiments require a basic understanding of HDL compilation process, the mapping between HDL statements and digital logic primitives, and involve the use of HDL for design entry, simulation, synthesis, verification, the use of various CAD tools, personal computers, FPGA based development boards, writing skills and teamwork.
Grading:  
A = 3.5–4.0 (90–100%), B = 3.0–3.4 (80–89%), C = 2.0–2.9 (70–79%),  
D = 1.0–1.9 (60–69%), F= 0.0 (0–59%)  

Homework: 10%  
Labs: 20%  
Midterm exam: 30%  
Final exam/project: 40%  

Outcome Coverage for ABET Criteria 3:  

a. **An ability to apply knowledge of mathematics, science, and engineering.**  
Labs, homework assignments, and the final project need basic discrete math knowledge, digital logic skills, and basic programming skills.  
b. **An ability to design and conduct experiments, as well as to analyze and interpret data.**  
Homework assignments, labs, and the final project require students to analyze the given design problems and implement solutions using VHDL programming, and then verify and debug experimentally the solution adopted. In addition, algorithm design skills are required.  
c. **An ability to design a system, component, or process to meet desired needs**  
Homework and laboratory experiments require students to analyze, design, evaluate, and improve programs that meet specified constraints.  
d. **An ability to function on multidisciplinary teams.**  
n/a  
e. **An ability to identify, analyze and solve engineering problems.** In doing homework assignments, labs, and a final project each team needs to identify, analyze and solve a number technical problems and challenges. Each technical problem to be solved appropriately requires a thorough analysis of problem and the design of adequate algorithms.  
f. **An understanding of professional and ethical responsibility**  
n/a  
g. **An ability to communicate effectively.**  
Each group member needs to communicate effectively in order to finish labs and final project successfully.  
h. **Understand impact of engineering solutions in a global, economic, environmental and societal context**  
n/a  
i. **Recognition of the need for and an ability to engage in lifelong learning.**  
The use of advanced CAD tools and the programming of logic devices such as FPGA are an ideal “vehicle” to appreciate the need for lifelong learning.  
j. **Knowledge of contemporary issues**  
Homework assignments, exams, and the final project need in depth understanding of VHDL and Xilinx software  
k. **An ability to use techniques, skills, and modern engineering tools necessary for engineering practice.**  
Project management skills are necessary to finish projects and homework assignments timely. In addition good programming skills and the adoption of precise programming guidelines shows the importance to continuously improve and refine the solutions given during consecutive labs and homework assignments.