This assignment addresses:

**Learning Objective #3:**

*Design application specific function units with HDL.* (Criteria 3a, 3b, 3c, 3e, 3i, 3j, 3k)

- Question A

**Learning Objective #1:**

*Demonstrate proficiency coding in HDL (Hardware Design Language).* (Criteria 3a, 3e, 3j, 3k)

- Question D

**Problem set 3**

Use VHDL to design and test a circuit that takes as input a serial bit stream and outputs a ‘1’ whenever the sequence “1111” occurs. Overlaps must also be considered, that is, if …001111110… occur than the output should remain active for three consecutive clock cycles.

Grading will be based on:
A. Correctness of the design [40 %]
B. Compliance with specifications [10 %]
C. Effectiveness of testing [40 %]
D. Coding style [10%]

Make sure to include:
- VHDL files
- Waveforms illustrating the behavior of the circuit. Comment the waveforms and illustrate that the system works as expected