Problem Set 3

Design, simulate, and synthesize the circuit described in Problem 8.2 [100 pts]
Make sure to include:
1. The VHDL developed for the circuit
2. The VHDL code developed to simulate the behavior of the circuit. Comment on the “quality/exhaustiveness” of your testing strategy waveforms illustrating the behavior of the circuit.
3. Waveforms illustrating the behavior of the circuit
4. A concise “commented” summary of the synthesis outcome.