This assignment addresses:

Learning Objective #2:

*Design basic functional units with HDL. (Criteria 3a, 3b, 3c)*

- Question A and C

Problem Set 1

Use VHDL to design and test a combinational circuit capable of comparing two 2-bit unsigned numbers A and B. The circuit must have three outputs AGTB, AEQB, and ALTB, corresponding to A>B, A=B, A<B, respectively.

1. Derive the truth table for the system and obtain the corresponding logic expressions in the sum-of-products format
2. Submit VHDL code for both design and testbench.
3. [Optional]
   Submit the waveforms used for testing. Comment the waveforms and make sure to illustrate that the system works as expected

Grading will be based on:

A. Correctness of the design [50 pts]
B. Compliance with specifications [10 pts]
C. Effectiveness of testing [40 pts]