This assignment addresses:

Course Learning Objective #5:

 Applies HDL to various application problems. (Criteria 3b, 3c, 3e, 3g, 3k)
  ● Question D

Course Learning Objective #2:

 Designs basic functional units with HDL. (Criteria 3a, 3b, 3c)
  ● Question A

Lab #4

The objective of this lab is to learn how to modify and re-use existing code. You are provided with the documentation and the VHDL code of a UART (universal asynchronous receiver/transmitter). One of the units composing the UART is a FIFO. However the original VHDL code of the FIFO coming with the UART is missing. Fortunately enough, you have available the code of another FIFO which is quite similar though not exactly the same. In order to reconcile the differences you will need to slightly modify the code of the UART. In addition to the UART’s code you are also provided with the VHDL code of a verification circuit that was devised for an FPGA prototyping board similar to the Spartan 3E, except for the fact that it mounts a 7 segments LEDs display rather than an LCD display. Modify the verification circuit so that you can implement it into your Spartan-3E Board.

Since you will need to reuse the UART for your final project, make sure to understand well every detail of the design.

The UART on the FPGA make it possible to interface the prototyping board with a PC. The electrical interfacing can be done using a straight-through serial cable connecting the RS-232 serial port of the PC and the one on the prototyping board (DCE connector). For further details see Chapter 7 of the Spartan 3E Starter Kit Board User Guide (pp. 59-60).
The UCF constraints for the DCE RS-232 port are:

NET "RS232_DCE_RXD" LOC = 'R7' | IOSTANDARD = LVTTL ;
NET "RS232_DCE_TXD" LOC = 'M14' | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = SLOW ;

**Figure 7-3: UCF Location Constraints for DCE RS-232 Serial Port**

1. Write a short professional quality report documenting the main characteristic and performance of the system you designed (think of the document as the “data sheet” of your system)
2. Submit VHDL code for both design and test.
3. Demonstrate the operation of the circuit on the prototyping board

Grading will be based on:

A. Correctness of the design [50 pts]
B. Coding style quality [20 pts]
D. Quality of the report [30 pts]