Lab #1

The goal of this lab is to get familiar with the usage of VHDL Simili (VHDL Simili is a VHDL Compiler and Simulator produced by Symphony EDA).

Use VHDL to design and simulate a muxed D flip-flop.

Write a short report including:
1) a true table of the system
2) vhdl code developed for the circuit
3) vhdl code developed to simulate the behavior of the circuit
4) waveforms illustrating the behavior of the circuit