Lab. 1

Design an NMOS current source to provide a bias current of $I_O=100 \ \mu A$ and an output resistance greater than $20\ \text{M}\Omega$. The reference current is to be $I_{\text{REF}}=150\ \mu A$. The circuit is to be biased at $+/-3.3\text{V}$ and the voltage at the drain of the current source transistor is to be no smaller than $-2.2\text{V}$.

Hint: NMOS transistors are available with the following parameters:
$V_{T_N}=0.5\ \text{V}$, $K'_n=80\mu\text{A/V}^2$, and $\lambda=0.01\ \text{V}^{-1}$