Homework #7

Problem 7.4 (5 pts)
Sketch the outputs of an S-R latch of the type shown in Figure 7.5 for the input waveforms shown in Figure X7.4. Assume that input and output rise and fall times are zero, that the propagation delay of a NOR gate is 10 ns, and that each time division below is 10 ns.

Problem 7.5 (5 pts)
Repeat Drill 7.4 using the input waveforms shown in Figure X7.5. Although you may find the result unbelievable, this behavior can actually occur in real devices whose transition times are short compared to their propagation delay.

Problem A (10 pts)
Show how to build a D flip flop using a T flip flop and combinational logic.

Problem B (10 pts)
Show how to build a J-K flip flop using a T flip flop and combinational logic.