ENGR430 - Sample Midterm Problems

Problem 1 [10 pts]
What does CMOS Stand for?

C =
M =
O =
S =

What does VLSI stand for?

V =
L =
S =
I =

What are the two main advantages of CMOS Technology over Bipolar Technology?

1.

2.

What are the conditions that must be verified for an nMOS transistor to work in the following mode?

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<thead>
<tr>
<th>Operation mode</th>
<th>Condition One</th>
<th>Condition Two</th>
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<tr>
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</tr>
<tr>
<td>Saturation</td>
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What are the conditions that must be verified for a pMOS transistor to work in the following mode?

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**Problem 2 [5 pts]**
Given the following planar capacitor with a voltage of $V_c = 1V$ applied to it,

1. How much charge $Q_c$ can be accumulated on its plates?
2. How much is the electric field $E_c$ across its dielectric? And what is the direction of the electric field?

Assume the material between the plates is silicon oxide?

![Capacitor Diagram]

The relative permittivity of silicon oxide is:

$\varepsilon_r = 4$

The permittivity of vacuum is:

$\varepsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$

<table>
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<th>value</th>
<th>unit</th>
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<tr>
<td>$Q_c =$</td>
<td>$\frac{1}{2}CV_c$</td>
<td>$\text{C}$</td>
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<td>$E_c =$</td>
<td>$\frac{V_c}{d}$</td>
<td>$\text{V/m}$</td>
</tr>
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</table>

The direction of the electric field is:
Problem 3 [10 pts]

In general the drain-to-source current of an nMOS transistor depends on the following parameters:
- Electrons Mobility
- Silicon Oxide permittivity
- Width of the transistor
- Length of the transistor
- Silicon oxide thickness
- Threshold Voltage
- Gate to Bulk Voltage
- Drain to Source Voltage

1. What is the equation of the drain-to-source current of an nMOS transistor in cut-off region:
   \[ I_{ds} = \]

2. How can the transistor be modeled in cut-off region?

3. What is the equation of the drain-to-source current of an nMOS transistor in triode-region for \( V_{ds} \ll V_{gs} - V_T \):
   \[ I_{ds} = \]

4. How can the transistor be modeled in triode region with \( V_{ds} \ll V_{gs} - V_T \)?

5. What is the equation for the drain-to-source current of an nMOS transistor in saturation region (neglect channel length modulation):
   \[ I_{ds} = \]

6. How can the transistor be modeled in saturation?
**Problem 4 [5 pts]**

List all intrinsic and parasitic capacitances of an nMOS transistor:

![nMOS transistor diagram]

Intrinsic:
1.
2.
3.

Parasitic:
4.
5.

**Problem 5 [5 pts]**

List at least 5 non ideal I/V effects that are neglected in the MOS “hand-derived” I/V equations:

1.
2.
3.
4.
5.
6.
7.
8.
Problem 6. [20 pts]

Consider an nMOS transistor. The inversion charge "accumulated" in a small section of the channel that goes from x to x+dx is given by:

\[ dQ(x) = \frac{\varepsilon_{ox}}{t_{ox}} \left[ V_{gs} - V_{th} - V(x) \right] W \cdot dx \] (1)

The electrical potential across the section is considered approximately constant and equal to V(x).

The current \( I_{ds} \) flowing through a section of the channel placed at the point x is given by:

\[ I_{ds} = \frac{dQ(x)}{dt} \] (2)

Since the average velocity of the electric charge flowing through a section of the channel placed at the point x is given by:

\[ \text{velocity}(x) = \mu \cdot E(x) = \mu \cdot \frac{dV(x)}{dx} \] (3)

The time \( dt \) taken for the electric charge to travel from x to x+dx is given by:

\[ dt = \frac{dx}{velocity(x)} = \frac{dx}{\mu \cdot \frac{dV(x)}{dx}} \] (4)

Substituting (3) and (4) in (1) and (2) we can write that:

\[ I_{ds} = \frac{\varepsilon_{ox}}{t_{ox}} \cdot \mu \left[ V_{gs} - V_{th} - V(x) \right] W \cdot \frac{dV}{dx} \]

Derive \( I_{ds} \) as a function of \( V_{gs} \) and \( V_{ds} \).
**Problem 7 [12 pts]**

Given a circuit, composed by two D-flip flops, a combinational logic block A and the following timing parameters:

- $T_{clk} = \text{clock period}$
- $T_{FF1} = \text{propagation delay of FF1}$
- $T_{su1} = \text{setup time of FF1}$
- $T_{h1} = \text{hold time of FF1}$
- $T_{FF2} = \text{propagation delay of d-FF2}$
- $T_{su2} = \text{setup time of FF2}$
- $T_{h2} = \text{hold time of FF2}$
- $T_A = \text{propagation delay of the logic block A}$

Derive the setup and hold time inequalities that must hold true in order for the circuit to work reliably.

1. Setup inequality:

2. Hold time inequality:

3. Assuming the circuit must reliably work in a range of Temperature that goes from -55 °C to 125 °C and a supply voltage range that goes from 2.97V to 3.63V, what values of Temperature and Voltage must be used to guarantees that setup and hold time constraints are verified.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Voltage Value [V]</th>
<th>Temperature Value [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Setup constraint</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hold Constraint</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Problem 8 [4 pts]
Given the following four circuits derive their output voltage $V_{out}$:

(a) $V_{DD}$

(b) $V_{out} = $

(c) $V_{out} = $

(d) $V_{out} = $
Problem 9 / 10 pts

CMOS Inverter Transfer Function

Given a CMOS inverter, specify in which mode the transistors work for each of the regions illustrated in the CMOS inverter Transfer Function

<table>
<thead>
<tr>
<th>Region</th>
<th>p-device operating mode</th>
<th>n-device operating mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
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<tr>
<td>C</td>
<td></td>
<td></td>
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<tr>
<td>D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
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</tbody>
</table>
**Problem 10 [6 pts]**
In CMOS technology, dynamic power dissipation is composed by two contributes:

\[ P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{short-circuit}} \]

1. What is the cause of \( P_{\text{switching}} \)?

2. What factors does \( P_{\text{switching}} \) depend on?

3. What is the cause of the \( P_{\text{short-circuit}} \)?

**Problem 11 [2 pts]**
Express the unit of measure of the inductance [Henry] in terms of Volt, Ampere, second. Show your work.
Problem 12 [5 pts]
Is the following circuit reliable? YES NO

Explain why?
**Problem 13 [10 pts]**

Given the following circuit estimate the RC propagation delay from A to Y when the input signal switches from low-to-high:

\[ t_{pd} = \frac{1}{\frac{1}{R} + \frac{1}{C}} \cdot RC \]
Problem 14 / 20 pts

a. Draw the CMOS transistor level schematic for a gate computing $F = (A+B) \cdot (C+D)$

b. Sketch the layout stick diagram of the gate $F = (A+B) \cdot (C+D)$
**Problem 15. [5 pts]**
If temperature increases, how does the drain-to-source current of an MOS transistor change? Select all true statements:

a. increase proportionally  
b. decrease proportionally  
c. increases but not proportionally  
d. decreases but not proportionally

Why? _________________________________________________________________

**Problem 16. [5 pts]**
If the supply voltage of a CMOS logic cell increases, how does the current charging the cell’s load changes? Select all true statements.

a. increases  
b. decreases

Why? _________________________________________________________________

**Problem 17 /5 pts**
Given the following two circuits derive their output voltage $V_{out}$:

(a) 
\[ V_{DD} \]

(b) 
\[ \text{GND} \]

\[ V_{out} = \]

\[ V_{out} = \]
**Problem 18 [10 pts]**

Given the following circuit estimate the propagation delay from A to Y when the input signal switches from low to high. [Propagation delay is defined as the time it takes the output voltage \( V_Y \) to reach the 50% of its final value].

Assume the output Y drives a capacitive load \( C_Y = 1 \)pF and that the pMOS transistor has a drain to source resistance \( R_p = 2 \) Kohm.

The length of the pMOS and nMOS transistor is the same, but the width of the pMOS transistor is 2 times the width of the nMOS transistor.

![Circuit Diagram]

\[ t_p = \]