ENGR 430 – Problem Set #2

This assignment addresses Course Learning Objective #1.

Analyze and design basic logic circuits that form the building blocks of a digital integrated system particularly with applications to combinational logic gates and sequential logic gates (ABET criteria 3a, 3c)

Problem #1
Using LTspice draw the transistor-level schematic of a CMOS compound OR-AND-INVERT gate implementing the following function:

\[ F = (A + B) \cdot C \]

Problem #2
Using LTspice draw the transistor-level schematic of a CMOS compound OR-OR-AND-INVERT gate implementing the following function:

\[ F = (A + B) \cdot (C + D) \]

Problem #3
Using LTspice draw the logic-level schematic of a CMOS positive edge triggered D flip-flop with asynchronous clear (use only inverters, 2-input nands, and transmission gates)